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Filing Date	April 28, 2004
First Named Inventor	DeVries
Art Unit	2811
Examiner Name	Im, J. M.
Attorney Docket Number	BUR920030184US1

ENCLOSURES *(Check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
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- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
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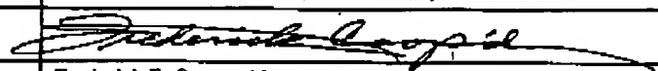
Signature			
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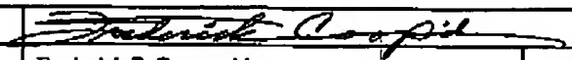
Signature			
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TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. BUR920030184US1

In Re Application Of: **DeVries, et al.**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/709,325	April 28, 2004	Im, J.M.	21254	2811	3324

Invention: **METHOD AND STRUCTURE FOR CONNECTING GROUND/POWER NETWORKS TO PREVENT CHARGE DAMAGE IN SILICON ON INSULATOR**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **October 25, 2006**

The fee for filing this Appeal Brief is: **$500.00**

☐ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

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Dated: **December 26, 2006**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of

DeVries, et al.

Serial No.: S/N: 10/709,325 Group Art Unit: 2811

Filed: April 28, 2004 Examiner: Im, J. M.

For: **METHOD AND STRUCTURE FOR CONNECTING GROUND/POWER NETWORKS TO PREVENT CHARGE DAMAGE IN SILICON ON INSULATOR**

Commissioner of Patents
Alexanderia, VA 22313-1450

APPELLANTS' BRIEF ON APPEAL

Sir:

Appellants respectfully appeal the rejection of claims 1-10, 19, and 20 in the Office Action dated July 25, 2006. A Notice of Appeal was timely filed on October 25, 2006.

I. REAL PARTY IN INTEREST

The real party in interest is International Business Machines Corporation, assignee of 100% interest of the above-referenced patent application.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or Assignee which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

Claims 1-10, 19, and 20 are all of the claims presently pending in the application. Claims 11-18 are withdrawn and are not part of this Appeal, but are subject to rejoinder. Claims 1-10, 19, and 20 stand rejected on prior art grounds.

Claim 19 stands rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,869,844 to Liu et al. Claims 1-6 and 8-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu, further in view of US Patent 6,329,391 to Finzi.

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu, further in view of US Patent 6,815,771 to Kimura. Claim 7 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu/Finzi, further in view of Kimura.

All these above-recited rejections are being appealed. Therefore, the rejections for claims 1-10, 19, and 20 are being appealed.

IV. STATUS OF AMENDMENTS

A Request for Reconsideration Under 37 CFR §1.116 was filed on September 25, 2006. In the Advisory Action mailed on October 19, 2006, the Examiner indicated that the arguments in the Amendment Under 37 CFR §1.116 were not persuasive and that the

rejections were maintained. The claims in the Appendix reflect the version of the claims of the Amendment Under 37 CFR §1.111 as filed on April 24, 2006.

V. SUMMARY OF CLAIMED SUBJECT MATTER

As described and defined in, for example, claim 1, the present invention is directed to an electronic chip including a first circuit design module having a first grid and a second circuit design module having a second grid. The first grid and the second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in the fabrication.

As explained beginning at paragraph [0039], the conventional practice in SOI circuit design and fabrication is that the various circuit design modules are interconnected in the final metallization step (e.g., M5).

The claimed invention, on the other hand, teaches that the charging due to plasma processing is not distributed uniformly over the two-dimensional surface of the chip. Therefore, the plasma processing can cause differential voltages across the chip, including, particularly, differential voltages between the grids of the various design modules on the chip.

As explained in paragraph [0032], the term "circuit design modules" refers to the different portions of a circuit designed by different engineering teams, typically quite visible by looking at the ground and/or voltage grids of the overall circuit. Conventionally, in SOI technology, no thought is given to the interconnection of these design modules until later metallization steps. The present inventors surmised that the failures they have noted

on SOI circuits might be due to a previously-unrecognized two-dimensional differential voltage during plasma processing that becomes noticeable for larger design modules not interconnected before the plasma processing step.

As discussed in paragraph [0009], conventional wisdom assumes that SOI is immune from such differential voltage breakdown. Thus, contrary to conventional wisdom, the present invention teaches that the design modules on SOI should be interconnected prior to the final metallization (or any other stage for which plasma processing will possibly cause a large two-dimensional differential voltage).

Independent Claim 1

1. (Rejected) An electronic chip (Paragraph [0015]; Figure 3, item 300) , comprising:

a first circuit design module (see various design modules 301-308 of Figure 3) having a first grid (e.g., grid 210 on Figure 2); and

a second circuit design module (see various design modules 301-308 of Figure 3) having a second grid (e.g., grid 212 on Figure 2),

wherein said first grid and said second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in a fabrication of said electronic chip, such that said first grid and said second grid do not accumulate an excessive differential voltage due to said plasma process (Figure 5 shows grids 501,502 interconnected by diffusion layer 505; Figure 6 shows grids 601,602 interconnected by gate structure 603; Figure 7 shows grids 701,702 interconnected by FET 703, where the silicon layer of the FET is considered conductive during plasma

processing; Figure 8 shows grids 801,802 interconnected by local interconnect 803 at a lower level; and Figure 9 shows grids 901,902 interconnected by a metal layer designed to matchup at the boundary 903 of the two design modules).

Independent Claim 19

19. (Rejected) An electronic apparatus [Paragraph 0017] comprising:

at least one electronic chip (303, Figure 3), comprising:

a first circuit design module (see various design modules 301-308 of Figure 3) having a first grid (e.g., grid 210 on Figure 2);

a second circuit design module (see various design modules 301-308 of Figure 3) having a second grid (e.g., grid 212 on Figure 2); and

means for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip (Figure 5 shows grids 501,502 interconnected by diffusion layer 505; Figure 6 shows grids 601,602 interconnected by gate structure 603; Figure 7 shows grids 701,702 interconnected by FET 703, where the silicon layer of the FET is considered conductive during plasma processing; Figure 8 shows grids 801,802 interconnected by local interconnect 803 at a lower level; and Figure 9 shows grids 901,902 interconnected by a metal layer designed to matchup at the boundary 903 of the two design modules).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Since Appellants appeal all rejections currently of record, Appellants present the following grounds for review by the Board of Patent Appeals and Interferences, as follows:

GROUND 1: THE REJECTION UNDER 35 USC §102(e) FOR CLAIM 19, AS BASED ON LIU;

GROUND 2: THE REJECTION UNDER 35 USC §103(a) FOR CLAIMS 1-6 AND 8-10, AS BASED ON LIU, FURTHER IN VIEW OF FINZI;

GROUND 3: THE REJECTION UNDER 35 USC §103(a) FOR CLAIM 20, AS BASED ON LIU, FURTHER IN VIEW OF KIMURA; and

GROUND 4: THE REJECTION UNDER 35 USC §103(a) FOR CLAIM 7, AS BASED ON LIU/FINZE, FURTHER IN VIEW OF KIMURA.

VII. ARGUMENTS

IN GENERAL

The examiner alleges that Liu anticipates claim 19, and, when modified by Finzi, renders obvious claims 1-6 and 8-10, and when modified by Kimura, renders obvious claim 20. The Examiner also alleges that further modification of Liu/Finzi by Kimura renders obvious claim 7.

On the continuation sheet in the Advisory Action dated October 19, 2006, the Examiner alleges: "*Applicants argue on page 8 that the instant invention has distinction*

over the prior art with the emphasis underlined. However, these aspects are not recited explicitly in the claims."

In response, Appellants submit that all the underlined features, relating to different grids, different design modules, interconnection before the plasma processing, and SOI are very clearly in the claims and that the Examiner simply ignores the plain meaning of the claim language.

As explained in paragraph [0037], the present invention teaches that the damage to the chip components is due to two-dimensional differences in charging during the plasma process, so that, as shown in figure 2, different surfaces of the chip will receive different amount of charges. Moreover, as explained in paragraph [0032] and illustrated in Figure 3, the present invention exemplarily defined by independent claim 19 is directed toward a chip 300 that has a plurality of grids resultant from respective design efforts of different engineering teams. These design grids might typically be power or ground grids, as described in dependent claims 3, 13. When these design grids are sufficiently large on chips, such as SOI (e.g., see paragraph [0036] and dependent claims 6, 7, 15, 16, and 20), that have a layer isolating the circuit layers from the substrate, the inventors have surmised that the reason for failures during fabrication is due to lateral differences in charging during plasma processing that shows up in these different design team grids.

Therefore, the present invention teaches that, to overcome the damage done by this unequal distribution of charges, the different grids of different design modules should be electrically interconnected before the first plasma operation after the grid has been formed. If these grids are not interconnected, as explained above, the plasma process can provide a

different distribution of charges on the different grids, thereby causing a differential voltage between the grids and potential damage to the circuits.

GROUND 1

Primary reference Liu does not address chips having circuits isolated from the substrate, such as SOI, and the mechanism in this reference is based upon providing a discharge path from a protected structure through a back-to-back diode connected in series to the substrate, as clearly described in lines 14-15, column 2, and lines 27-29, column 3.

More important, the protective device in Liu is directed to the gates of a line of transistor devices, to provide a dissipation path to the substrate, much in the manner described by the background discussion in paragraph [0008] of the disclosure of the present invention. There is no indication in Liu of a "first circuit design module" and a "second circuit design module", as this terminology is discussed and described in paragraph [0032] of the disclosure. This terminology in the claims refers to the different portions of a circuit designed by different engineering teams, as clearly illustrated in Figure 3. The discussion in primary reference Liu is directed to protecting a line of gates, not a "design module", as required by the claim language.

Therefore, relative to claim 19, even if the line of gates shown in Figure 2 of Liu were to be considered a "grid", the primary reference still fails to satisfy the plain meaning of the claim language, since the only protective mechanism in Liu is to the substrate and involves only the single grid. There is no mechanism that protects against a differential accumulation of charges across two grids that are isolated from the substrate, since the mechanism in Liu will inherently discharge to the substrate before a differential charge

between the grids builds up. Nor is there any suggestion to provide an interconnection between two design modules.

Stated slightly differently, even if these two features 12, 14 were to be considered as "grids", the protective mechanism in Liu is only for the second grid 12 but not for the first grid 14 and that protective mechanism discharges to the substrate. There is no electrical interconnection between grids 12 and 14 in Liu.

Finally, relative to the Examiner's refusal to provide patentable weight to " ... no later than a first metalization layer of said chip" and "... a plasma processing", Applicants submit that the claim wording does indeed define a structure that is detectable in the finished product and, therefore, is not processing designation that has no patentable weight, as alleged by the Examiner. That is, the finished product includes two or more grids, readily observable by one of skill in the art as indicative of a design module, and these grids will be electrically interconnected with an actual structure that will be observable by one of ordinary skill in the art.

As clearly explained in MPEP §2173.01: "*A fundamental principle contained in 35 U.S.C. 112, second paragraph is that applicants are their own lexicographers. They can define in the claims what they regard as their invention essentially in whatever terms they choose so long as the terms are not used in ways that are contrary to accepted meanings in the art. Applicants can use functional language, alternative expressions, negative limitations, or any style of expression or format of claim which makes clear the boundaries of the subject matter for which protection is sought. As noted by the court in* In re Swinehart, 439 F.2d 210, 160 USPQ 226 (CCPA, 1971), *a claim may not be rejected*

solely because of the type of language used to define the subject matter for which patent protection is sought."

To one having ordinary skill in the art, the structure interconnecting two grids of two design modules is readily determinable as having been fabricated in a step prior to one in which a plasma processing might be used. Therefore, as such, this wording does indeed have patentable weight, since such structure can be detected by one having ordinary skill in the art in a potentially infringing device.

The Examiner's reliance on *In re Thorpe* is misplaced, since the description in MPEP §2113 does not imply that the wording of a claim related to process is simply ignored. Rather, this description requires that any "... *structure implied by the process steps should be considered* ...."

Appellants submit that this requirement in MPEP §2113 to consider structure clearly contradicts the characterization in the rejection that all wording related to process can be simply ignored as allegedly having no patentable weight. As explained above, the language of the independent claims, even if considered as related to a fabrication process, clearly involves structure and such structure cannot simply be ignored in the prior art evaluation as allegedly having no patentable weight.

Hence, turning to the clear language of the claims, in Liu there is no teaching or suggestion of: "... a first circuit design module having a first grid; a second circuit design module having a second grid; and means for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip", as required by claim 19.

GROUND 2

Relative to the rejection for claims 1-6 and 8-10, the same deficiencies identified above for claims 19 apply equally well to independent claim 1. Liu has not been demonstrated as resultant from two design modules, as clearly required by the plain meaning of the claim language, and only one of the two "grids" identified in the rejection has a protection mechanism. There is no electrical interconnection between the two grids.

The Examiner concedes that primary reference Liu fails to teach or suggest the claim limitation that the two grids do not accumulate excessive differential voltage due to plasma processing and relies upon secondary reference Finzi. The Examiner further alleges that one having ordinary skill in the art would have been motivated to modify Liu by Finzi "... *in order to have a protection circuit wherein two grids do not accumulates (sic) an excessive voltage due to the plasma process to improve a data speed.*"

Appellants submit that, to one having ordinary skill in the art, this rationale is a *non-sequitur* since there is no logical connection between data speed and installing another protection circuit in primary reference Liu. Therefore, Appellants submit that this rejection fails to provide a motivation to modify the primary reference and, thus, fails to meet the initial burden of a *prima facie* rejection for obviousness. Appellants submit that Finzi is also similar to the discussion in paragraph [0008] of the disclosure, wherein a device is provided with a protective diode for protection during fabrication. Finzi, therefore, does not overcome the basic deficiencies previously discussed for primary reference Liu.

Hence, relative to independent claim 1 and turning to the clear language of the claims, in Liu there is no teaching or suggestion of: "... a first circuit design module having

a first grid; and a second circuit design module having a second grid, wherein said first grid and said second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in a fabrication of said electronic chip, such that said first grid and said second grid do not accumulate an excessive differential voltage due to said plasma process."

Moreover, Appellants submit the following deficiencies in the rejection currently of record for the following dependent claims:

- relative to claim 6, the circuit in Liu is fabricated in the substrate, so that, in contrast to the SOI structure, there will inherently be substantial leakage of current in Liu; and

- relative to claim 9, the Examiner is respectfully requested to identify the discussion in Liu that supports any concern about surface area.

GROUND 3

Primary reference Liu is not an SOI structure, as required by dependent claim 20. Appellants submit that one having ordinary skill in the art recognizes that SOI is a technology quite distinct from the substrate technology of Liu and that Liu, therefore, cannot simply be converted into SOI without changing its principle of operation and, more significantly, the principle of operation of its mechanism to provide a discharge path to the substrate.

That is, in the rejection, the Examiner attempts to modify the technique in primary reference Liu, based on non-SOI technology, to incorporate the SOI structure of Kimura

and alleges that one would be motivated to "... *incorporate the teachings of Kimura into the device of Liu in order to have said chip including a silicon on insulator (SOI) structure to alleviate the problem of breakdown voltage.*"

However, Appellants submit that modification of Liu to convert it into SOI would change the underlying principle of operation of its protective mechanism, since this mechanism requires a path to the substrate, and SOI would preclude such path. Therefore, such conversion would be improper since it would defeat the purpose of the mechanism in the primary reference.

Thus, Appellants submit that the rejection for claim 20 fails to meet the initial burden for a *prima facie* rejection since the rejection of record improperly attempts to simply change the chip of primary reference Liu into an SOI chip, thereby clearly and improperly changing its principle of operation.

GROUND 4

Appellants submit that the rejection for claim 7 has the same deficiencies identified for claim 20, as discussed for Ground 3.

Therefore, Appellants submit that there are elements of the claimed invention that are not taught or suggest by Liu, Finzi, or Kimura, and the Board is respectfully requested to withdraw these rejections.

VIII. CONCLUSION

In view of the foregoing, Appellants submit that claims 1-10, 19, and 20, all the claims presently pending in the application, are clearly patentably distinct from the prior art of record and in condition for allowance. Thus, the Board is respectfully requested to remove all rejections of claims 1-10, 19, and 20.

Please charge any deficiencies and/or credit any overpayments necessary to enter this paper to Assignee's Deposit Account number 09-0456.

Respectfully submitted,

Dated: 12/26/06

Frederick E. Cooperrider
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APPENDIX

Claims, as reflected upon entry of the Amendment Under 37 CFR §1.111, filed on April 24, 2006, are as follows.

1. (Rejected) An electronic chip, comprising:

a first circuit design module having a first grid; and

a second circuit design module having a second grid,

wherein said first grid and said second grid are interconnected in a fabrication layer no later than a first metallization layer of said chip that accumulates a charge during a plasma process in a fabrication of said electronic chip, such that said first grid and said second grid do not accumulate an excessive differential voltage due to said plasma process.

2. (Rejected) The electronic chip of claim 1, wherein at least one of said first grid and said second grid comprises a metallization grid.

3. (Rejected) The electronic chip of claim 1, wherein said first grid and said second grid respectively comprise one of a power grid and a ground grid.

4. (Rejected) The electronic chip of claim 1, wherein said first grid and said second grid are interconnected by at least one of:

a diffusion region;

a gate of a field effect transistor;

a source of a field effect transistor connected to said first grid and a drain of said field effect transistor connected to said second grid;

a local interconnect; and

a metallization layer that is designed to electrically interconnect at a boundary of said first circuit design module and said second circuit design module.

5. (Rejected) The electronic chip of claim 1, wherein an interconnect between said first grid and said second grid is conductive during said plasma processing and is non-conductive during an operation of said chip unless activated by a signal.

6. (Rejected) The electronic chip of claim 1, wherein said chip comprises components fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip.

7. (Rejected) The electronic chip of claim 6, wherein said chip includes a silicon on insulator (SOI) structure.

8. (Rejected) The electronic chip of claim of claim 6, wherein said layer is temporarily activated by said plasma processing such that carriers in said layer are migratable during said plasma processing.

9. (Rejected) The electronic chip of claim 2, wherein at least one of said first grid and said second grid comprises a metal grid that includes a predetermined surface area of at least one of said first circuit design module and said second circuit design module.

10. (Rejected) An electronic apparatus comprising:

an electronic chip fabricated in accordance with claim 1.

11. (Withdrawn) A method of at least one of designing an electronic chip and fabricating said electronic chip, said method comprising:

interconnecting at least one grid of a design module of an electronic circuit formed on said chip with a corresponding grid in a second design module in a stage of fabrication of said chip such that a plasma processing of said fabrication does not cause a differential charge that damages a component of said chip.

12. (Withdrawn) The method of claim 11, wherein at least one of first grid and said second grid each comprise a grid formed by metallization.

13. (Withdrawn) The method of claim 11, wherein said first grid and said second grid comprise one of a power grid and a ground grid.

14. (Withdrawn) The method of claim 11, wherein said first grid and said second grid are interconnected by at least one of:

a diffusion region;

a gate of a field effect transistor;

a source of a field effect transistor connected to said first grid and a drain of said field effect transistor connected to said second grid;

a local interconnect; and

a first metallization layer that is designed to electrically interconnect at a boundary of said first circuit design module and said second circuit design module.

15. (Withdrawn) The method of claim 11, wherein said chip comprises components fabricated in a layer that has substantially no leakage of carriers to a substrate of said chip.

16. (Withdrawn) The method of claim 15, wherein said chip comprises a silicon on insulator (SOI) structure.

17. (Withdrawn) The method of claim of claim 11, wherein said layer is temporarily activated by said plasma processing such that carriers in said layer are migratable during said plasma processing.

18. (Withdrawn) The method of claim 12, wherein at least one of said first grid and said second grid comprises a metal grid that is a predetermined surface area of at least one of said first circuit design module and said second circuit design module.

19. (Rejected) An electronic apparatus comprising:

at least one electronic chip, comprising:

a first circuit design module having a first grid;

a second circuit design module having a second grid; and

means for electrically interconnecting said first grid and said second grid no later than a first metallization layer that accumulates a charge during a plasma process in a fabrication of said chip.

20. (Rejected) The electronic apparatus of claim 19, wherein at least one of said at least one electronic chip comprises a chip including a silicon on insulator (SOI) structure.

EVIDENCE APPENDIX

(NONE)

RELATED PROCEEDINGS APPENDIX

(NONE)